SUBJECT: A Transistorized Variable Delay Unit

TO: ~~Kenneth H. Olsen~~ GROUP 63 STAFF

FROM: Leonard Kleinrock

DATE:

APPROVED: _____ BEN GURLEY

ABSTRACT: ~~This note describes a~~ THIS transistorized variable delay unit ~~which~~ converts a negative pulse into a 3 volt negative level whose width is adjustable over a range from 0.3~~0~~ microseconds to ~~10~~ 2.5 seconds. Greater widths may be obtained by adding capacitance externally. When loaded with 100 ohms the output level is -2.9 volts, fall time is ~~0.11~~ 0.09 microseconds, and rise time 0.03 microseconds. A compensating circuit for voltage drift is included which maintains the delay width constant within less than 0.5% for a 10% variation in any supply voltage. Jitter is below 0.2%.

DISTRIBUTION LIST:

Maybe the output should be a delayed 5134 inverted because this may be a standard output ckt. ?

TABLE OF CONTENTS:

INTRODUCTION:

This variable delay unit supplies a negative level of variable duration when supplied with a negative pulse at the input. Many desirable features are built into it and its reliability is EXPECTED TO BE quite high. This unit will supply a 100 ohm resistive load with a -2.9 volt level whose fall time is 0.09 microseconds and whose rise time is 0.03 microseconds. Jitter is kept down to less than 0.2%. The output pulse width may be varied continuously over the entire range of 0.3 microseconds to 2.5 seconds with 5 coarse positions. Longer delays are easily obtained by adding capacitance externally at the terminals provided. The output pulse width is affected only slightly by supply voltage variations, e.g. for a 10% change in any supply voltage, the width changes by less than 0.5%.

DEVELOPMENT:

As a first attempt in solving the problem of designing a variable delay unit, a monostable multivibrator was investigated. The emitter coupled type was eliminated because of its undesirable output pulse level, i.e., the output swing is not from ground level to -3 volts. The collector coupled monostable multivibrator showed more promise. However the following difficulties were encountered. Referring to Figure 1, note that the delay time is directed proportional to the product of R_1C. However, the maximum value of R_1 is limited because the d-c base current for transistor Q2 must flow through R_1. If we desire a long delay time we will therefore find it necessary to increase the value of C. This brings us to a second difficulty, namely, that the recovery time (which is proportional to the product R_2C), becomes excessive. These problems were overcome by placing an emitter-follower between R_2 and C as well as between R_1 and the base of transistor Q2. This circuit however introduced too much delay time during the regeneration period (transition period) which resulted in a slower output waveform than could be acceptable.

It was ~~next~~ decided that a monostable multivibrator which depends upon internal delay for its proper functioning would not be suitable, ~~for our purposes.~~ AND SO ~~Therefore~~, a circuit using external delay was investigated. As shown in Figure 2, a flip-flop was used which was triggered ON by the input pulse and triggered OFF, after a time interval BY A SIGNAL FED BACK FROM THE OUTPUT ~~as determined by the~~ RC timing circuit. ~~It was found that~~ the set one pulse coming from the timing circuit was too slow to give a suitable trailing edge to the output waveform, AND SO ~~Therefore~~ an emitter coupled bistable multivibrator, also known as a Schmitt circuit, was added, as shown dotted in Figure 2. This provided an extremely fast set one pulse. A Schmitt circuit responds only when the input signal exceeds a minimum amplitude, which is known as the triggering level. This triggering level is sensitive to supply voltage drifts, and therefore in an attempt to compensate for such drifts the Schmitt circuit was supplied from the same voltage sources as was the RC timing circuit. This greatly reduced the sensitivity of the delay width to supply voltage drifts. Basically this is the form of the FINAL ~~present~~ circuit. Further improvements are described below.

CIRCUITRY AND OPERATION: → FIG 4 ON NEXT FULL PG.

A block diagram and a circuit schematic of the variable delay unit are shown in Figures 3 and 4 respectively. ~~In the quiescent state, the output is at ground potential.~~ When a negative pulse arrives at the input terminal, the collector of Q2 and ~~also~~ of Q3 are both pulled toward ground, from -3 volts. This starts the transition of the flip-flop which results in the collector of Q3 remaining at ground potentialand the collector of Q4, as well as the output terminal shifting to the -3 level. The output pulse has now started. The base of Q6 is now pulled to ground which cuts off this transistor. The voltage across C up until this time had been 0 volts due to the clamping action of Q6. Now that Q6 has been cut off the potential at ~~point A~~ ITS COLLECTOR begins to rise from -3 volts toward +10 volts. The rate of rise ~~is~~ IS inversly proportional to the product of RC. The emitter-follower, Q7, follows directly with the rising voltage at ITS BASE. ~~point~~ A. Q6 and Q7 comprise the timing circuit. The signal is now fed into a drift compensating circuit which functions as follows.

IN DETAIL, THE CIRCUIT OPERATION MAY BE DESCRIBED AS FOLLOWS. IN THE QUIESCENT CONDITION, ~~STATE,~~ ~~THE~~ ASSUME THAT THE FLIP-FLOP IS IN THE 1 STATE (THIS IS VERIFIED FURTHER ON), SETTING THE OUTPUT AT GROUND POTENTIAL.

The assumption is made that transistor Q8 does not conduct until its emitter potential equals or exceeds the potential of its base, at which time Q8 with its associated load resistor act as a standard inverter type circuit. In Figure 5 is shown a plot of the voltage at the emitter of Q8 versus time. Here the assumption is made that this waveshape is linear, whereas it is known that this is an exponentially rising waveform. This assumption is valid since we are dealing only with a small portion of this waveform at its beginning where it is nearly linear. In this Figure, E volts represents the absolute difference between the +10 and -3 supply voltages. Line AB represents the waveshape for a +10 supply voltage of value +10 volts. Assuming, for the moment, that the base voltage is fixed at a level which we shall call trigger level one, it is seen that at time t_1, the inverter will start to conduct. Assume now that the supply voltage drops by an amount delta E as shown in Figure 6 at point C. Line AC now represents the waveshape at the emitter of Q8. The intersection of this line and trigger level one, occurs at a time t_2 which is greater than the desired time T1. One way to compensate for this change in time is to change the trigger level from trigger level 1 to trigger level 2 which will then cause the intersection to occur at time t_1. By similar triangles it is seen that,

$$\frac{\text{trigger level 2}}{\text{trigger level 1}} = \frac{E - \Delta E}{E}$$

Therefore,

$$\text{trigger level 2} = \left[\frac{E - \Delta E}{E}\right] \text{trigger level 1}$$

This gives us the value of the new desired trigger level. One obvious way to set this new trigger level is to put the base of Q8 at this new level. This may be accomplished automatically by connecting Q8 as shown in Figure 7. From our orginal assumption we have defined the base voltage to be the trigger level. For the condition where the +10 supply voltage is equal to E volts, the trigger level is therefore equal to,

$$\text{trigger level 1} = \left[\frac{R_1}{R_1 + R_2}\right] E.$$

If now the supply voltage changes by a quantity - ΔE the new trigger level will be

$$\text{Trigger level 2} = \frac{R1}{R1 + R2}\left[E - \Delta E.\right]$$

Combining these two equations they see that,

$$\text{trigger level}_2 = \left[\frac{E - \Delta E}{E}\right] \text{trigger level 1}$$

By comparing this trigger level 2 to the desired trigger level 2 as determined from Figure 5, we see they are identical, and have thereby compensated for the change in the +10 supply voltage. By superposition, a change in the -3 V supply as well as in the change in the +10 supply will also be compensated for in the identical manner. NOTE THAT THE VALUES OF R_1 AND R_2 DO NOT ENTER INTO THE FINAL EQUATIONS, AND MAY THEREFORE DRIFT WITHOUT CONSEQUENCE. THEY HAVE BEEN CHOSEN TO FALL WITHIN THE OPERATING RANGE OF Q_8.

The collector of Q8 will start rising at a time determined only by the setting of R and C and not dependent upon the supply voltage level. The inverting action thru Q8 also has associated with it a large gain which effectively amplifies the slope of the waveform at its emitter. This signal is then raised roughly 3 1/2 volts through the Zener diode and appears at the base of Q9 which is the input to the Schmitt circuit.

The base voltage of Q9 is held clamped at a potential determined by the constants of the Schmitt circuit, the Zener diode, and the 5.6 K resistor. Therefore the collector of Q8 is clamped at a potential roughly 3.5 volts negative of this. When the collector of Q8 begins to rise the base of Q9 rises with it at higher level. The Schmitt circuit is set to trigger at a voltage roughly 1 volt positive of its clamped voltage. When the Schmitt circuit triggers, the collector of Q10 sharply rises from about -1.8 volts to a level slightly above ground, which cuts off Q2. This triggers the flip-flop and forces a transition to take place. The output at Q5 now swings from its -3 V level to the ground level which thereby terminates the output pulse.

The recovery time of the circuit is quite short. The longest recovery time is associated with C, and this has conveniently been minimized by allowing C to recharge through the collector current of Q6.

VARIATIONS IN THE -15V SUPPLY ALTER THE DELAY TIME BY AFFECTING THE QUIESCENT BASE VOLTAGE OF Q_9. HOWEVER, BY ADDING THE 12K RESISTOR FROM THIS SUPPLY TO THE BASE OF Q8, A CORRECTING SIGNAL IS GENERATED WHICH COMPENSATES FOR SUCH DRIFTS.

In summary the operation of the circuit is as follows. A negative input pulse is applied to the input trigger stage. This triggers the flip-flop and sends the output from ground level to -3 level. At the same time this initiates a timing circuit, which is compensated for supply voltage drifts, and allows a time interval to pass during which the output is held at the -3 level. At the end of this time interval the Schmitt circuit is triggered which in turn triggers the flip-flop. The flip-flop then goes through a second transition returning the output to the ground level. The width of this output pulse is thereby determined by the setting of R and C only.

PERFORMANCE:

Figure 7 shows photographs of the waveforms at critical points in the circuit. The delay time was arbitrarily set at 10 microseconds. Note the linear rise in voltage at the base of Q7, and the amplified slope of this rise at the input to the Schmitt circuit.

As is the practice with such circuits a number of margin check plots were made which proved quite satisfactory, giving wide margins for variations in the important parameters.

Further data in this respect may be found in Lincoln Laboratory Computation Book Number 1307.

SPECIFICATIONS AND RANGE

1. Input: Requires a negative pulse whose minimum amplitude is -1.5 volts and whose duration should be at least 20% less than that of the desired output pulse.

2. Output: specifications:

   (a) Minimum delay time: 0.3 microseconds,

   (b) Maximum delay time: 2.5 seconds.

   Note: Longer delays may be obtained by adding external capacitance at the terminals provided.

   (c) Fall time unloaded: 0.05 microseconds
   Rise time unloaded: 0.03 microseconds.
   Fall time loaded with 100 ohms: 0.09 microseconds
   Rise time loaded with 100 ohm: 0.03 microseconds.

   (d) Output swing unloaded: -3 volts.
   Output swing loaded 100 ohms: -2.9 volts.

THE ASSUMPTION MADE IN THE THIRD PARAGRAPH OF THIS SECTION MAY NOW BE VERIFIED. IF THE FLIP-FLOP WERE TO REMAIN IN THE 0 STATE, THE TIMING CIRCUIT WOULD BEGIN FUNCTIONING (SINCE Q_6 WOULD BE CUT OFF), AND THIS WOULD BE FED THROUGH TO THE SCHMITT CIRCUIT, WHICH WOULD ~~BE FORCED~~ TRIGGER. ONCE TRIGGERED, THE COLLECTOR OF Q_9 JUMPS ~~POSITIVE~~ ABOVE GROUND POTENTIAL, AND THIS IS FED TO THE BASE OF Q_2 WHICH MUST THEREFORE STOP CONDUCTING. IF Q_2 IS NOT CONDUCTING, THE FLIP-FLOP MUST SWITCH TO ITS 1 STATE, Q.E.D.

NOTE ALSO THAT THE QUIESCENT LEVEL AT WHICH THE OUTPUT SIGNAL SETTLES IS ~~GROUND~~ A FEW TENTHS OF A VOLT ABOVE GROUND. THIS ALLOWS DIRECT COUPLING TO A TRANSISTOR BASE, WITHOUT ADDING POSITIVE BIAS. IT MAY ALSO BE SEEN THAT THE 100 OHM LOAD ~~IS CHOSEN~~ HARDLY ALTERS THE OUTPUT SWING.

FIGURE 8 SHOWS THE VARIATION IN OUTPUT PULSE WIDTH AS A FUNCTION OF THE SUPPLY VOLTAGES, FOR A PULSE WIDTH OF 100 MICROSECONDS. NOTE THAT WITHIN $\pm 10\%$ CHANGE IN SUPPLY VOLTAGE, THE PULSE WIDTH REMAINS CONSTANT WITHIN $\pm 0.5\%$.

3. Maximum pulse repetition frequency at minimum delay time: 3 megacycles
4. Jitter: 0.2%
5. Supply voltages: +10, -3, -15. Note: This circuit ~~has already~~ also ~~been designed~~ for operation at -10 instead of -15 volts.
6. Semi-conductors required: 7 Philco type L-5122 transistors, 3 Philco type L-5134 transistors, 1 ~~Zener diode type~~ _____.
7. Delay range:

Delay Position	R	C	~~Delay Range~~
Position 1	1K-100K	470 MF	0.35 microseconds - 5.5 microseconds
Position 2	"	.01 MF	2 microseconds - 100 microseconds
Position 3	"	.22 MF	35 microseconds - 2 milliseconds
Position 4	"	6 MF	1 milliseconds - 60 milliseconds
Position 5	"	180 MF	20 milliseconds - 10 secnnds.

NOTE: WHEN ADDING ~~CAPA~~ EXTERNAL CAPACITANCE TO OBTAIN LONGER DELAYS, PUT A 47Ω RESISTOR IN SERIES WITH THE CAPACITOR TO LIMIT ~~FREQUENT~~ EXCESSIVE CURRENTS.

Include R&C for each range

8— additional pg.

FIGS 7 & 8 ON LAST 2 PGS.

8-

Polarity of Output Signal:

The circuit described in this note gives an output that is ~~normally~~ quiescently at ground ~~level~~ potential, and then drops to -3 volts ~~throughout the duration of the pulse, finally returning to ground at the~~ for the duration of the pulse. If desired, an output may be obtained which normally supplies a -3v level, & rises to ground potential for the duration of the pulse. This may be accomplished by ~~connecting~~ feeding the output into a clamped inverter (for low power applications) or into an inverter-cascode combination (for higher power applications) as is used in the TX-2 Computer circuits.